CLAIMS

What is claimed is:

1. An adaptive analog equalizer that operates on a signal, comprising:

a high pass network and a multiplier, the multiplier has an adjustable gain that is adjusted using gain control;

the high pass network and the multiplier have a frequency response that, when adaptively applied to an input signal, are operable to compensate for corruption in the input signal;

the gain control uses an output of the adaptive analog equalizer to adjust the adjustable gain of the multiplier; and

the high pass network and the multiplier modify the input signal, the modified input signal is summed with the input signal.

2. The adaptive analog equalizer of claim 1, wherein the input signal comprises a channel corrupted input signal.

3. The adaptive analog equalizer of claim 1, wherein the input signal is provided from a communication channel, the communication channel having a channel frequency response; and

the frequency response of the high pass network and the multiplier is substantially an inverse of the channel frequency response.

4. The adaptive analog equalizer of claim 1, wherein the gain control performs decision and sampling control of the output signal; and

the gain control integrates an output signal from the decision and sampling control using an integrator.

5. The adaptive analog equalizer of claim 1, further comprising a variable gain amplifier, an integrator, and a peak detector; and

wherein the output signal is passed through the peak detector and the integrator to provide a control signal for the variable gain amplifier.

6. The adaptive analog equalizer of claim 1, wherein the adaptive analog equalizer performs double sampling of the input signal.

7. The adaptive analog equalizer of claim 1, wherein the adaptive analog equalizer waits a first predetermined period of time after detecting a pulse rising edge before sampling a first sample of the input signal; and

the adaptive analog equalizer waits a second predetermined period of time after detecting the pulse rising edge before sampling a second sample of the input signal.

8. A double sampling adaptive analog equalizer, comprising:

a gain control unit comprising a decision and sampling control circuit, the decision and sampling control circuit is operable to perform double sampling of an input signal; and

the gain control unit comprises a gain control processed feedback loop that forces the input signal to a predetermined value within a bit period after detecting a pulse rising edge.

9. The double sampling adaptive analog equalizer of claim 8, wherein the decision and sampling circuit waits a first predetermined period of time after detecting the pulse rising edge before sampling a first sample of the input signal.

10. The double sampling adaptive analog equalizer of claim 9, wherein the first predetermined period of time is less than a pulse period.

11. The double sampling adaptive analog equalizer of claim 8, wherein the decision and sampling circuit waits a second predetermined period of time after detecting the pulse rising edge before sampling a second sample of the input signal.

12. The double sampling adaptive analog equalizer of claim 11, wherein the second predetermined period of time is greater than a pulse period.

13. The double sampling adaptive analog equalizer of claim 8, wherein the predetermined value is zero.

14. The double sampling adaptive analog equalizer of claim 8, wherein the adaptive analog equalizer structure comprises a high pass network and a multiplier having an adjustable gain.

15. The double sampling adaptive analog equalizer of claim 14, wherein the input signal is provided from a communication channel, the communication channel having a channel frequency response; and

a frequency response of the high pass network and the multiplier is substantially an inverse of the channel frequency response.

16. A method to perform analog adaptive equalization, the method comprising:

detecting a pulse rising edge of an input signal;

waiting a first predetermined period of time after detecting the pulse rising edge before sampling a first sample of the input signal;

waiting a second predetermined period of time after detecting the pulse rising edge before sampling a second sample of the input signal; and

adjusting a gain of a multiplier when the second sample does not exceed a predetermined threshold.

17. The method of claim 16, wherein the first predetermined period of time is less than a pulse period.

18. The method of claim 16, wherein the second predetermined period of time is greater than a pulse period.

19. The method of claim 16, wherein the input signal comprises a channel corrupted input signal.

20. The method of claim 16, further comprising forcing the input signal to zero within a bit period after detecting the pulse rising edge in response to a one to zero transition.